

# Resume of Prashant Ramrao Deshmukh

Address : Associate Professor and Head  
Department of Electronics and Telecommunication  
Engineering  
Government college of Engineering,  
Amravati-444 604

Tel : 09423610594 (Mobile)

E-mail : pr\_deshmukh@yahoo.com, [pr\\_deshmukh@ieee.org](mailto:pr_deshmukh@ieee.org)

## **Education:**

Doctor of Philosophy in Engg and Technology (Ph.D.), 2005

Master of Engineering (M.E.), 1997

Bachelor of Engineering (B.E.), 1988

Diploma in VLSI Design (ACTS CDAC, Pune), 2001

Advance diploma in Computer software and system Analysis  
(A.D.C.S.S.A.A.), 1991

## **Software/Hardware Skills Summary :**

HDL Programming,  
Assembly language programming  
Digital system design,  
Microprocessor/Microcontroller Based system Design  
PC based Interfacing,  
Digital Signal Processing, Image/Video Processing  
Data Mining

## **Work Experience:**

32 year Teaching experience,

## **Supervisor For ME , PhD ( No of students Guided ) :**

- M.E. : 32 Students
- PhD : 11 Students (awarded)

### **Membership:**

1. Life Member of Indian society for Technical Education (LM 10898).
2. Fellow of Institute of Electronics' and Telecommunication Engineers (IETE F-133100).
3. Life Member (Fellow) of Institute of Engineers (M-119535/7, F-114024-4).
4. Life Member of Instrument society of India(M-1193).
5. Senior Member of IEEE (M-8056743)
6. Life Member, Computer Society of India( M-00165055).

### **Other Responsibilities:**

1. Member, Board Of studies (Computer Science and Engg) S.G.B. Amravati University, Amravati.Since from 2007 to 2012.
2. Member, Board of Studies (Electrical Engg) , Member on Faculty of Engineering , S.G.B. Amravati University, Amravati.Since from 2012 to 2017.
3. Joint secretary, Alumni association of Government College of Engineering, Amravati in 1999-2002.
4. Executive Member and Life Member of Alumni association of Government College of Engineering, Amravati.
5. Executive Member of IETE Amravati Local center, 2005-2010 , Vice president for 2010-2012 and worked as chairman of IETE Amravati centre for period 2012 to 2014...
6. Faculty Advisor, ISTE Student chapter.
7. University Recognized PhD Supervisor For Electronics /Computer Science & Engg /Information technology (SGBAU/554/181/2007 Dt. 26/07/2007, RTMNU- PhD cell/RRC/Guide/2260/B/1004,18.04.2012,/SGBAU/554/295/2008,Dt 16/09/2008 ,IT-10/2014 dated 20.01.2014 )
8. Worked as chairperson in National level Paper and Project completion , PAROKSHA 2011,5-7 March 2011, at Raison College of Engg and Management, Amravati.
9. Worked as a Resource person in A 2 week AICTE-ISTE approved course on “ VLSI system Design and Applications “at PRMIT, Badnera, 22 March 2007.
10. Worked as chairperson in National level Paper and Project completion , Technospeak 2010, 20th Aug , at HVPM COET ,, Amravati
11. Conducted one day workshop on “ Embedded system Goverment Polytechnic, Amravati on 25<sup>th</sup> March 2011.
12. Worked as Convener for National level National level Technical symposium “Vidyotan 2009” in Jan 2009.
13. Worked as Convener for National level National level Technical symposium “Vidyotan 2008” in Sept 2008.
14. Worked as Cordinator for Two week AICTE-ISTE Approved STTP on “open source applications/ from 28th Dec 2009 to 1<sup>st</sup> Jan 2010.
15. RBTE Representative, over board of studies (Electronics and Telecommunication) at Govt Polytechnic, Amravati since from 2011.
16. Conducted one day workshop on “Microcontroller and applications” at SSBT College of Engineering and Technology Jalgaon at 8<sup>th</sup> sept 2012.
17. Chair person in International conference on Emerging Trends and and Research in Engineering and Technology at IBBS Engg Amravati on 6<sup>th</sup> April 2015.
18. Chair person in International Conference on Science and Engg at Birla Institute of Technology Dubai UAE, from 21<sup>st</sup> to 23<sup>rd</sup> November 2015.

19. Worked as Convener for National level National level Technical symposium “Adhayaa 2018” in Feb 2018.
20. Dean (Quality Assurance) since from 2017.

**Rating of Appraisal:** Excellent in last five years

**Awards:**

1. Best Teacher award for Maharashtra state, From Indian society for Technical Education(ISTE) , New Delhi in 2003.
2. Eminent Engineer Award form Institute of Engineers(India), Amravti center in 2004.
3. ISTE-Rajaram Bapu Patil Narional Award For promosing Engineering Teacher for creative work done in Technical Education 2007
4. National level “IETE-Prof K. Shreenivasan Memorial Award 2011” for his outstanding contribution for institutional Development
5. ISTE-U.P. Government National Award 2011 for Outstanding work done in area of Rural-oriented and socially relevant development activity .
6. Best Teacher Award from Govt. of Maharashtra 2012-13
7. Life time Achievement Award in International Conference for Outstanding contribution in Filed of Engineering and Technology held at Birla Institute of Technology Dubai UAE, on , 21<sup>st</sup> to 23<sup>rd</sup> November 2015
8. Late Horoji Ulemale Award for Outstanding contribution in Technical education by Shri Shivaji education Soicety, Amravati in 2014.

**Ph.D.Supervisor: ( 11 students ,PhD awarded)**

1. Efficient performance Evaluation of a Novel Universal algorithm for Noise reduction in Image Denoising ( Student : M.V. Sarode Awarded in 2013).
2. Study of Hamming Distance Based Polygram substitution cipher algorithm for coding optimization in data communication (Student: A.S. Joshi, Awarded 2014)

3. Study of Ternary Logic applications in the design of Low power Asynchronous circuits (Student : V.T. Gaikwad, Awarded in 2016)
4. Novel topology control architecture for Large wireless sensor Network design and Its optimization (Student : D.R. Dandekar, Awarded in 2016)
5. Active Warden and Definite Minimal Requisite Fidelity for eliminating Covert Communication in TCP/IP (Student : D.M. Dakhane, awarded in 2016)
6. Gait Based Human Identification System by Silhouette analysis using region variance feature extraction through rectangular behavior (Student : P.B. Shelke, awarded in 2016)
7. “Construction of multifarious secret sharing scheme with Augmented capabilities (Student : Miss Sonali Patil awarded in 2016)
8. Novel adaptive and incremental learning algorithm for Support vector Machine (Student : Roshani Ade, awarded in 2016 )
9. “ Development of concurrent Architecture of vedic Multiplier –An accelerator scheme for High speed Computing” (Student: J.S. Edle , awarded in 2018)
10. “A Novel Load Balancing Algorithm” (Student: P.A. Tijare, awarded in 2018)
11. “A performance Analysis of Motion Vector Estimation Techniques for Imaging system” (student: Sandip T. Dighadi, Pursuring)
12. “An efficient scheduling algorithm for real time system with energy Harvesting” (Student: G.S. Thakare awarded in 2018)

**M.E. Supervisor:**

1. Design and Implementation of Floating point unit and Evaluation for FPGA (Student : Miss A.S. Deshmukh, awarded in 2009)
2. Design and Implementation of Low power ternary combinational circuits using ternary switches (Student :Miss K.S. Dhanokar awarded in 2009)

3. Implementation of Network Intrusion Detection system using Layered approach ( Student: Miss S.S. Kausik awarded in 2010)
4. Non-preemption scheduling of periodic and sporadic tasks on uniprocessor (student : G.S Thakare awarded in 2010)
5. Implementation of performance evaluation of web catching” (Student: H.N. Datir awarded in 2010).
6. “Cosine modulated Wavelet based texture features for content based Image retrieval” (Student: G.B. Regulawar awarded in 2010 )
7. Short Boundary Detection using automatic threshold (student: Sandip Dhagadi, awarded in 2012)
8. Fast and efficient detection of crack like defects in digital images (Students: Rashi Deshmukh, awarded in 2012)
9. Cluster Oriented Image Retrieval System (student: M.M. Bartere, awarded in 2012)
10. Intelligent Pattern Recognition System With Applications For Crop Disease Identification and Classification (student: Ms. Mrunalini R. Badnakhe , awarded in 2012)
11. Soft computing techniques for categorization of Unstructured Data (Student: Sonali Deshpande, awarded in 2012)
12. Texture Image retrieval using new rotated complex wavelet filters (Student: Mahulakar : Pursuing)
13. Implementation of Image inpainting for removal and region filling (Student: Rashmi Bijwe, awarded in 2012)
14. VLSI Implementation of DWT ( Miss S.R. Tavhare, awarded in 2012)
15. Design and Implementation of MAC (Student: Miss V.N. Choudhari : awarded in 2013)
16. “Multiple countries coin reorganization and identification using genetic algorithm” (Student: Miss Ashwini U. Dakhode , awarded in 2013 )
17. “Analysing Intrusion Detection using Machine learning Algorithm” (Student: Shazeba Kazi : awarded in 2013 )

18. "An effective implementation of Image secret sharing scheme (Student: Miss Arti Ghule : awarded in 2013 )
19. "Implementation of Data security in cloud computing" (Student: Miss Snehal Wasnaker : awarded in 2013 )
20. "Handwriting Analysis based on segmentation method for prediction of human personality using support vector machine" (Student: Aniket A. Raut : awarded in 2015 )
21. "Robust affine invariant feature extraction for image matching" (Student: Suraj Dhole : awarded in 2013)
22. "An efficient reserve AODV Routing protocol in MANET" (student: Ms Sujata Wankhade, Awarded in 2014)
23. "Multi Route AODV ant Routing Protocol in MANET (Student :Ashwini G. Choudhari, Awarded in 2014)
24. "An approach towards Information Extraction Based on Partitioning" (student: Ms. Sonam S. Chauhan, awarded in 2014).
25. "Hash Based Significant Bit Techniques For Video Steganography" (Stdeunt : Ms, Bhayashri D. Rhanagdale, awarded in 2014)
26. "Image segmentation road shape analysis from road sign recognition" (student: Ms. Ragini N. Choduahri, awarded in 2014)
27. "Optimum Tropical Cyclone Eye Fix using Genetic algorithm" (student: Ms. Pallavi Mathurkar, Awarded in 2014)
28. "Cache Updation Designing Behavior using Dynamic Source Routing Protocol" (student: Ms. Chaitali Taral, Awarded in 2014)
29. "Secure Hash Scheme for Image Authentication" (student: Ms. Smarudhi kulkar, Awarded in 2014)
30. "An Efficient Protocol for Privacy-Preserving Association Rule Mining" (Student: Prajkata Jaswante, awarded in 2016)
31. " An Efficient Protocol for Privacy-Preserving Association Rule Mining" (Student: Ruchita Sonar, awarded in 2015)

32. “An efficient Image fusion algorithm based on wavelet transform using Swarm Optimization Techniques”(Student : Ashivin W Hote, Awarded un 2017)

**Programmes/ Short term courses Completed/Attended :**

1. A 1-week course on "Logic Analyzer and Its applications" at G.P. Amravati during 7.6.99 to 11.6.99
2. A 2 - week AICTE-ISTE approved course on "Microcontroller and Electric Drives " held at G.P. Amravati during 14.9.98 to 25.9.98
3. A 4-week "Induction Phase-I" course at G.P. Amravati during 17.6.96 to 12.7.96
4. A 4-week "Induction Phase-II" course at G.P. Amravati during 04.08.97 to 30.08.97
5. A 4-week ISTE approved course on " Foundation course in computer applications (Module-I) at DR. P.D. Polytechnic, Amravati during 20.11.96 to 17.11.96
6. 3-days program on "Institutional Management " at Dr. P.D. Polytechnic, Amravati during 25.8.94 to 27.8.94
7. 1 week course on " 16 –bit Microprocessor Architecture and programming " at G.P. Amravati During 8.6.98 to 12.6.98
8. A 2-week AICTE-ISTE approved course on " Digital computer Networks “ at College of engineering, Badnera during 17.10.2002 to 30.10.2002 .
9. A 2-week AICTE-ISTE approved course on " Wavelet based computer graphics and Image processing “ at Amrita Institute of Technology and Science, Coimbatore during 20.01.2003 to 31.01.2003.
10. A National seminar on “VLSI System, Design and Technology” at IIT, Mumbai, December 9-11, 2000
11. A 2-Day workshop on "Matlab for Engineering applications: at S.S.G.M.C.E. Shegaon ,Februry 23<sup>rd</sup> to 24<sup>th</sup> 2002.
12. A 2 week AICTE-ISTE approved course on “ VLSI system Design and Applications “at PRMIT, Badnera
13. Participated in One day workshop “Restructuring the curriculum & Scheme for UG Courses” in Sant Gadge Baba Amaravti University, Amravati on 16/10/2008 at BNCOE Pusad.
14. Participated in Two days workshop “Restructuring the curriculum & Scheme for UG Courses” in Sant Gadge Baba Amaravti University, Amravati on 6<sup>th</sup> & 7<sup>th</sup> Aug 2008 at Sipna COET, Amravati
15. Participated in One day National conference on” Engineering Education” at PIET Pune, on dated 12.02.2005
16. 3 day workshop on”Total quality Mangment“ organized by Asian institute of quality management pune on 20-22 dec 2007 at Sipna COET Amaravti.
17. 1-week AICTE-STTP workshop on “ VLSI & Embedded system “ Organised by Electronics and Telecommunication Deptt, JDIET Yotomal 5/10/2009 to 9/10/2009.
18. 1 week Faculty development workshop orgniased by Sipna college of Engineering and Technology, from 22/10/2009 to 25/10/2009.

19. Trainners Empowerment Program By Face lift Foundation COET 19-24 Oct 2009
20. ISTE approved "Open source Application " at Sipna's C.O.E.T on 28<sup>th</sup> Dec–1<sup>st</sup> Jan 2010
21. Participate in one day workshop on " Restructuring of M.E. (Digital Electronics ) syllabus SGB Amravati University ogganised by PRMIT & R Badnera on 16<sup>th</sup> April 2010.
22. One day Training Programme for Teachers organized by S.G.B.A.U. and CDEEP, IIT Bombay on Aug 8, 2009.
23. One week AICTE-ISTE Approved short term training program on" Recent Trends in Artificial Intelligence" organized by JDIT Yeotmal from 10<sup>th</sup> to 14<sup>th</sup> Nov 2008.
24. Two days UGC Sponsored workshop on "Development and Implementation of Question Bank" Organized by S.G.B.A.U. on 30<sup>th</sup> and 31<sup>th</sup> March 2007.
25. Participated in one day work shop on Zero Error RAC at MSBTE Mumbai on 22Oct 2011.
26. One day workshop on NPTEL orgained by IIT Bombay and Viday Parsark mandal COE Bramati on 18<sup>th</sup> Sept 2014.
27. One week workshop on "Recent Treands in power Electronics, Drives and storage Technologies for Emerging applications" at VJTI Mumbai 5<sup>th</sup> to 9<sup>th</sup> Oct 2015.
28. Two week ISTE approved STTP on " Big Data anlystucs: A New Paradigm" at Sipna COET Amravati 20<sup>th</sup> to 30<sup>th</sup> April 2015
29. One week STTP on" Application to signal Processing : A system approach" at RGIT Amravati 13<sup>th</sup> Oct 2015 to 17<sup>th</sup> Oct 2015
30. One week AICTE Approved STTP on " Digital Signal processing and Design issues in VLSI OF Image processing " from 26/09/2017 to 10/10/2017 at Sipna College of Engineering and Technology ,Amravati.
31. One week DTE approved STTP on " Advanced computational tools in Engineering & Technology" from 19<sup>th</sup> March 2018 to 23<sup>rd</sup> March 2018 at Government College of Engineering , Nagpur.
32. One week DTE approved STTP on " Intellectual Property Rights " from 5<sup>th</sup> March 2018 to 9<sup>th</sup> March 2018 at Government College of Engineering , Nagpur.
33. One week DTE approved STTP on " Development of Green Campus " from 20<sup>th</sup> Feb 2018 to 24<sup>th</sup> Feb 2018 at Government College of Engineering , Nagpur
34. One week DTE approved STTP on " Disaster Management :Risk Assessment & Mitigation " from 12<sup>th</sup> March 2018 to 16<sup>th</sup> March 2018 at Government College of Engineering , Nagpur
35. Three Day Faculty Development Programme "Empowering academic excellence with overview of Industry 4.0 " from 21<sup>st</sup> Dec 2017 to 23<sup>rd</sup> Dec 2017 at Sipna College of Engineering, Amravati in collaboration with College of Engineering, Pune.



**Patent /Copy right**

<b>Patents</b>			
<b>Sr. No.</b>	<b>Title</b>	<b>Application Number</b>	<b>Application Status</b>
1.	Concurrent Architecture of Vedic Multiplier-An Accelerator Scheme for High Speed Computing	3315/MUM/2015	Published 11/09/2015
2.	Device and Interface for Ternary Logic Using VLSI Tool	4359/MUM/2015	Published
3.	Device Detection System	201621011604	Published
<b>PCT</b>			
<b>Sr. No.</b>	<b>Title</b>	<b>Application Number</b>	<b>Application Status</b>
1.	Concurrent Architecture of Vedic Multiplier-An Accelerator Scheme for High Speed Computing	PCT/IN2016/000117  Publication No WO2017037729A1	Published, 09/05/2017
2.	Device Detection System	PCT/IN2016/000128	Published
<b>Copyright</b>			
<b>Sr. No.</b>	<b>Title</b>	<b>Application Number</b>	<b>Application Status</b>
1.	VLSI Lab Manual	11745/2015-CO/L	Registered
2.	Development of Vedic Multiplier Architecture	10207/2017-CO/L	Registered
3.	Active Warden and Definite Minimal Requisite Fidelity For Eliminating Covert Communication in TCP/IP	18755/2017-CO/L	Registered
4.	Multi Valued Logic Applications in the design of Switching Circuits	1796/2018-CO/L	Registered
5.	An Efficient Scheduling Algorithm for Real Time System With Energy Harvesting.	2599/2018-CO/L	Registered

**Papers Published:**

<b>Journals</b>		<b>Conferences</b>		<b>Total (As on 1<sup>st</sup> Jan 2018)</b>
<b>International</b>	<b>National</b>	<b>International</b>	<b>National</b>	
88	14	46	73	221

**Note:** For actual paper, please search name (Dr P R Deshmukh ) in Google scholar